# Residential Scale AC Micro-Grid

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## 1. Our Proposal

The goal of this project is to provide students and faculty with a platform for testing micro-grid control schemes for power systems. The primary objective of this project is to design and construct a residential scale grid-like environment with a programmable load and multi-source capabilities. The ability to integrate renewable energy sources to the grid is challenging, and the proposed micro-grid test bed aims to provide solutions to these challenges. This project is designed to demonstrate how renewable sources can be used not only for supplemental generation, but also as a useful tool in improving common issues that are present in current AC grids. To this effect, various educational demonstrations will be prepared to illustrate the benefits associated with adding alternative sources, specifically solar energy, to the grid. The topics for demonstration include: grid synchronization, maximum power point tracking, power factor correction, unbalanced load compensation, and nonlinear load compensation.

The project has four stages of implementation: construction of the test bed hardware, testing and implementing controls systems for the micro-grid, integration of the test bed into the existing distribution system for our DOE Solar Decathlon building (known as the "Phoenix House"), and developing university course materials and educational demonstrations for students at all academic phases.

## 2. Overall Design

The hardware and software utilized in this project are all custom developed, which allows us to put into practice all of the control schemes for a micro-grid system. The primary focus of the hardware development has been on the inverter design, which is intended for use on each potential input to the micro-grid, including photovoltaic and battery sources. The inverter is designed as approximately a 2.5[kW] DC:AC device with integration to low-level control systems. This phase of the design utilizes two of these inverters.

*Figure 1: Phoenix House*

One of the inverters being used is the Grid-Emulating inverter, which uses the existing electrical service from the Phoenix House, as see in Figure 1, to create a three-phase AC grid. The second inverter will be fed from an existing photovoltaic (PV) service on the roof of the Phoenix House. Another piece of the hardware development is the programmable load, which includes a three phase resistive load, a three phase resistive-inductive load, and a nonlinear rectifier load with an ultra-high crest factor. The total load is designed to be approximately 5[kW] in size and features the ability to create unbalanced load conditions. The software is designed to implement various power system level controls systems, such as maximum power point tracking (MPPT) for the PV inverter, frequency regulation, and power factor correction. A high level system topology can be seen in Figure 1.

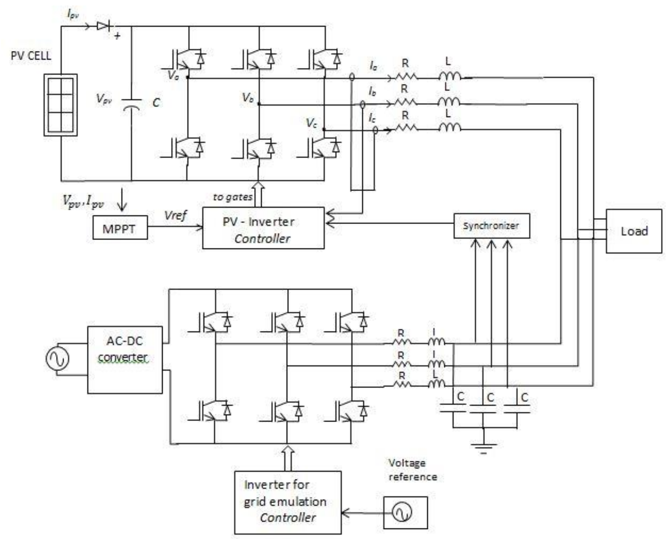


*Figure 2: Inverter Schematic*

## 3. Project Approach

The project has been developed through two student groups: graduate students and Capstone students. The focus of the graduate students has been on the PCB hardware development, which has entailed circuit design, simulation validations, and physical implementation of hardware and software. The focus of the capstone students was on the integration of the micro-grid test bed into the electrical distribution of the Phoenix House along with mechanical design of the micro-grid test bed. This group also worked on the project from a system engineering perspective, developing drawings along with bills of materials for different aspects of the project.

This report is organized as follows. In section 4, the high level system design will be covered, and section 5 will go over the low level hardware design. Sections 6 and 7 will cover the Capstone students' contributions, which are the thermal management and electrical distribution, respectively. Section 8 will discuss the physical implementation of the test bed, and section 9 will cover the control design associated with the system.

## 4. System Design

The project will create a 3-phase AC distribution system as described in Table 1. Our intention is to create a 3-Phase distribution bus that has a voltage magnitude with the capabilities of loading standard residential loads. With this, the system can also load standard AC appliances. A trade off analysis was completed that lead to our selection as seen in Table 1.

*Table 1*

| System Specifications | | |
|---|---|---|
| L-N Voltage | 110 | Vrms |
| L-L Voltage | 190.5256 | Vrms |
| Frequency | 60 | Hz |

The specification for the Grid-Emulating Inverter is shown in Table 2. The breaker shown is for the distribution feed from the Phoenix House, which will be covered in section 7. Table 3 shows the specifications for the PV inverter. The specifications for the Programmable Load is shown in Table 4. Note that each inverter is capable of running the RL load by itself, and when both inverters are active a combinations of these loads can be tested.

*Table 2*

| Grid-Emulating Inverter Specs | | |
|---|---|---|
| Minimum DC Bus | 311.127 | V |
| AC Input Voltage | 240 | Vrms |
| Voltage Doubler? | 1 | 1=N, 2=Y |
| Actual DC Bus | 339.4113 | V |
| Minimum Power* | 2269.976 | W |
| AC Input Current | 9.458234 | Arms |
| Breaker Current | 20 | Ap |
| Switching Frequency | 10 | kHz |
| Filter Inductance | 10 | mH |
| Filter Capacitance | 100 | uF |
| *based on RL load + single-phase R load for unbalanced load conditions | | |

*Table 3*

| PV Inverter Specs | | |
|---|---|---|
| Minimum DC Bus | 311.127 | V |
| Lowest PV Voltage* | 341.1 | V |
| Switching Frequency | 10 | kHz |
| Minimum Power** | 2626.47 | W |
| Filter Inductance | 10 | mH |
| *based on PV array MPP voltage | | |
| **based on maximum PV array power | | |

*Table 4*

| RL Load (delta) | | | | | |
|---|---|---|---|---|---|
| Desired | | | Actual | | |
| Total Load Power | 2000 | W | Total Load Power | 1906.976 | W |
| per-Phase | | | per-Phase | | |
| Load Power - P | 666.6667 | W | Load Power - P | 635.6587 | W |
| power factor | 0.94 | | power factor | 0.935715 | |
| Apparent Power - S | 709.2199 | VA | Apparent Power - S | 679.3292 | VA |
| Reactive Power - Q | 241.9677 | VAR | Reactive Power - Q | 239.6377 | VAR |
| Impedance | 51.183 | Ohms | Impedance | 53.43506 | Ohms |
| Current | 2.149151 | Arms | Current | 3.565554 | Arms |
| Resistance | 48.11202 | Ohms | Resistance | 50 | Ohms |
| Reactance | 17.46233 | Ohms | Reactance | 18.84956 | Ohms |
| Inductance | 0.04632 | H | Inductance | 0.05 | H |

| R Load (delta) | | | | | |
|---|---|---|---|---|---|
| Desired | | | Actual | | |
| Total Load Power | 1200 | W | Total Load Power | 1089 | W |
| per-Phase | | | per-Phase | | |
| Load Power | 400 | W | Load Power | 363 | W |
| Current | 2.099456 | Arms | Current | 1.905256 | Arms |
| Resistance | 90.75 | Ohms | Resistance | 100 | Ohms |

| Rectifier Load | | | | | |
|---|---|---|---|---|---|
| DC Voltage*** | | | | 278.55 | V |
| Desired | | | Actual | | |
| Load Power | 500 | W | Load Power | 517.2674 | W |
| DC Current | 1.79501 | A | DC Current | 1.857 | Arms |
| Resistance | 155.1802 | Ohms | Resistance | 150 | Ohms |
| Crest Factor* | 3 | | Crest Factor*** | 3.210738 | |
| Capacitance** | ? | uF | Capacitance | 680 | uF |
| Ripple Current** | ? | Arms | Ripple Current*** | 3.392 | Arms |

## 5. Low-Level Design

The functional block diagram for our inverter design is shown in Figure 2. Our approach is to divided up the circuit into four printed circuit boards (PCB). In the university environment, students troubleshooting skills are limited and this approach allows us to limit the scope of a circuit's function to a smaller element. Once a single board is functioning, then we can move to the next circuit to get that element working. This scheme is also beneficial when components fail as a large PCB needs to be replaced when a single sub-circuit fails. With this approach, only a small, in-expensive PCB can be replaced.

The first board (PCB1) is home to a common mode choke, used to filter the high-power AC input. Included on this board is a 15[A] fuse for overcurrent protection, along with X and Y capacitors for

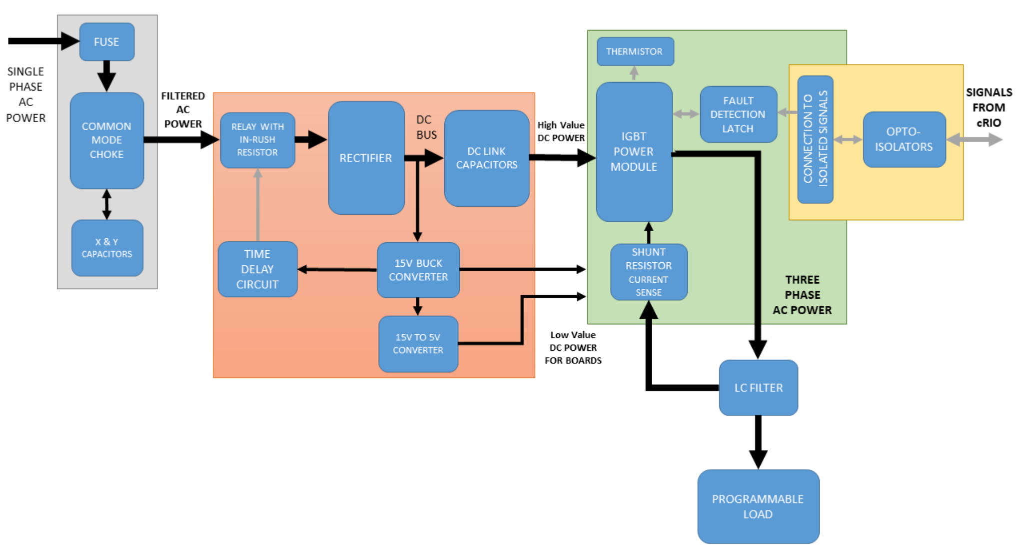


*Figure 3: Inverter Block Diagram*

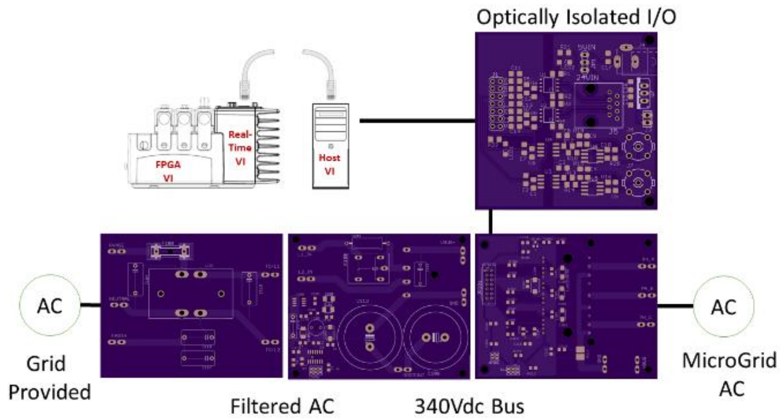


*Figure 4: Inverter Board Layout*

additional filtering. The second board (PCB2) is primarily for a full bridge rectifier to create the DC-Link for the subsequent Inverter PCB. PCB2 also has an in-rush current protection circuit that is comprised of a relay and a timer. Also on this board is a series of DC-DC converters that provide low-level DC power to both the relay circuit on this board, as well as any ICs on the following boards.

The third board (PCB3) utilizes an integrated-power module for the 3-phase DC:AC inverter. Paired with this power module is a shunt resistor that is used to feedback the output current, which the module can use to detect overcurrent conditions. A latch circuit has been designed to prevent the module from resuming operation in the event of a system fault.  The power module has all the necessary gate drivers required to control the hex-bridge. The final board (PCB4) contains a set of opto-isolators, which provides isolated signals from the system controller to the gate drivers of the inverter. For this project we use the National Instruments cRio 9066, see Figure 4.

The aforementioned design is intended for use as the Grid-Emulating inverter, and can be used for a 240 [Vrms] single-phase AC source. Sources that are DC in nature, such as PV panels, will simply omit the PCB1 in their design. PCB2, however, is still a necessary inclusion as the DC-DC converters are required to power the ICs on the final two boards (PCB3 and 4).

## 6. Thermal Management

The accumulation of heat in an electronic circuit is potentially damaging to electronic devices. Overheating can shorten the life expectancy of costly electrical components or lead to catastrophic failures. Using heat sinks in electronic circuits is very important to dissipate this thermal energy. In our project we used three methods to calculate the correct size of the heat sink. These three methods were based on the specific power module and diode rectifier and their operating conditions:

a. Generate a spreadsheet to calculate the power losses of the power module and rectifier circuit,
b. Use STLabMath software, which was provided from the power module manufacture, and
c. Implement the complete circuit in PLECS software, and use the thermal blocks inside the software.

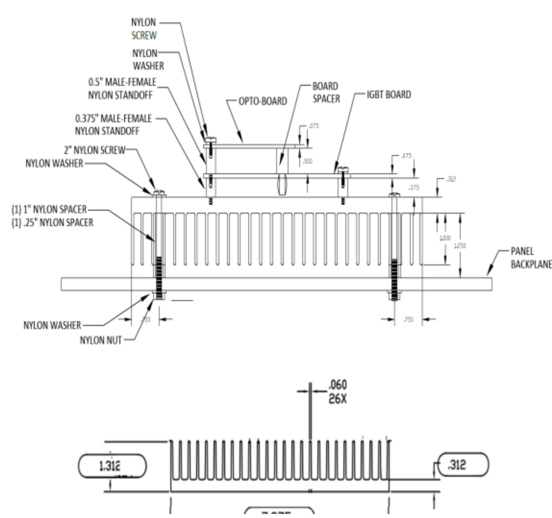


*Figure 5: Heat Sink Drawing*

The next step will be to mount the heat sink in its enclosure as outlined in section 9, and check the efficiency of the heat sink. Figure 5 shows the dimensions of the selected heat sink and the side and top views of the orientation.  Additional details are available upon request.

### 7. Electrical Distribution

The Capstone group developed a package outlining the integration of the micro-grid system with the existing electrical distribution present at the Phoenix House. This design package includes safety constraints based on NEC ratings regarding the construction and installation of the system. Figure 6 shows the three line diagram of the micro-grid system.  The system is tied into the existing distribution network through a 20[A] breaker rated at 240 [Vrms]. This will be connected to the micro-grid through a 208/240[V] split-phase transformer rated for 7.5[KVA].  The Phoenix house has a string of twenty-seven 300[W] PV panel on its roof.  A design requirement given to the Capstone group was to develop control circuity that will allow for connection of a portion of the PV panels to be connected to our system through contactors with integration into our system controller as seen in Figure 3.  This control circuity can be seen in Figure 6.

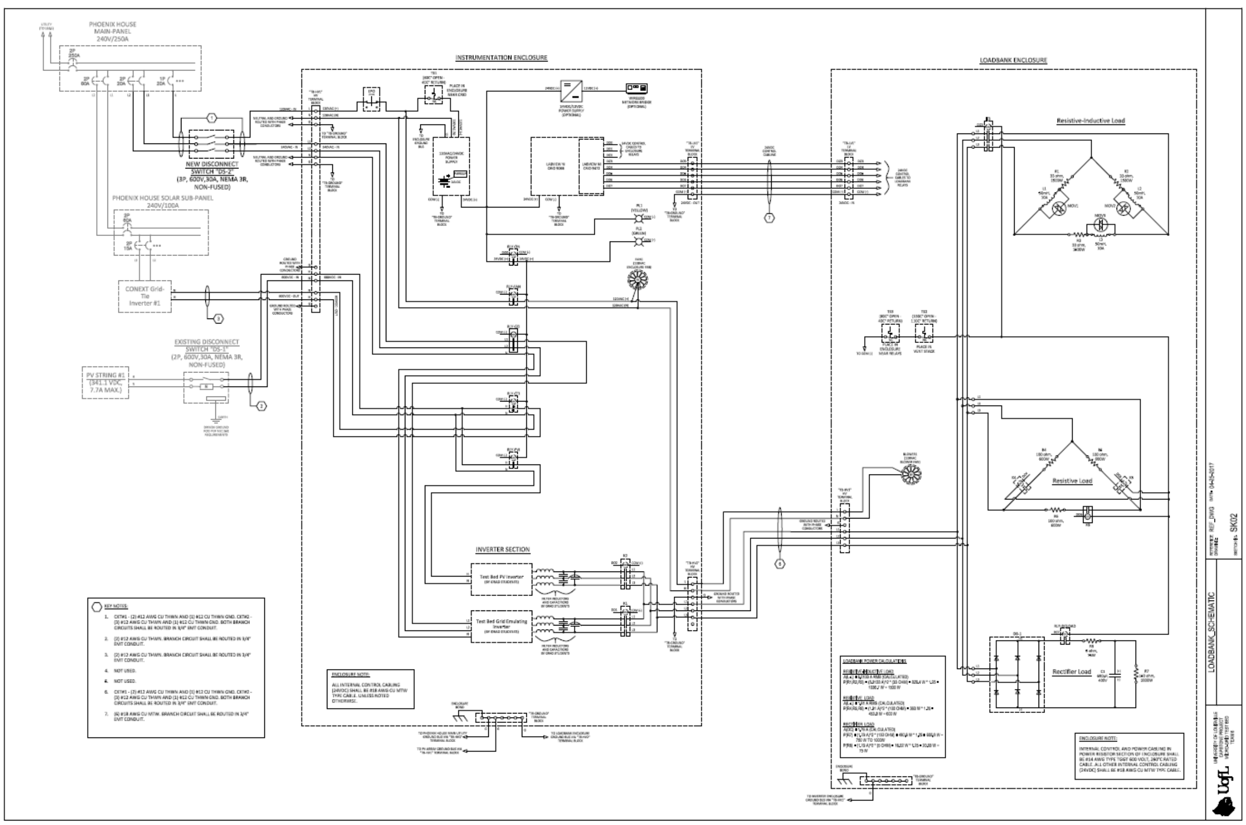


*Figure 6: Micro-Grid Three Line Diagram*

## 8. Physical Implementation

The Capstone students also complete a system level design for the physical implementation of the micro-grid test bed. For their design, they selected a two electrical panel layout. Panel 1, referred to as the Controls Enclosure is specified as a 30" x 36" x 8" outdoor electrical enclosure to house a controls power supply, switching relays/contactors, LabVIEW control components, test bed inverters on printed circuit board (PCB) packages, an air circulation fan, power and controls cabling and terminal blocks, etc. The enclosure was selected to be NEMA 4 rating to provide a weather proof seal to protect internal electronic components. An internal back plate/panel shall be included within the enclosure for mounting of electrical components.

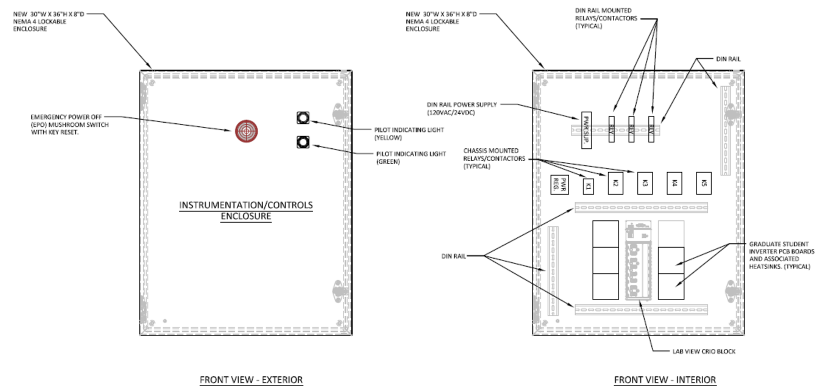


*Figure 7: Controls Enclosure*

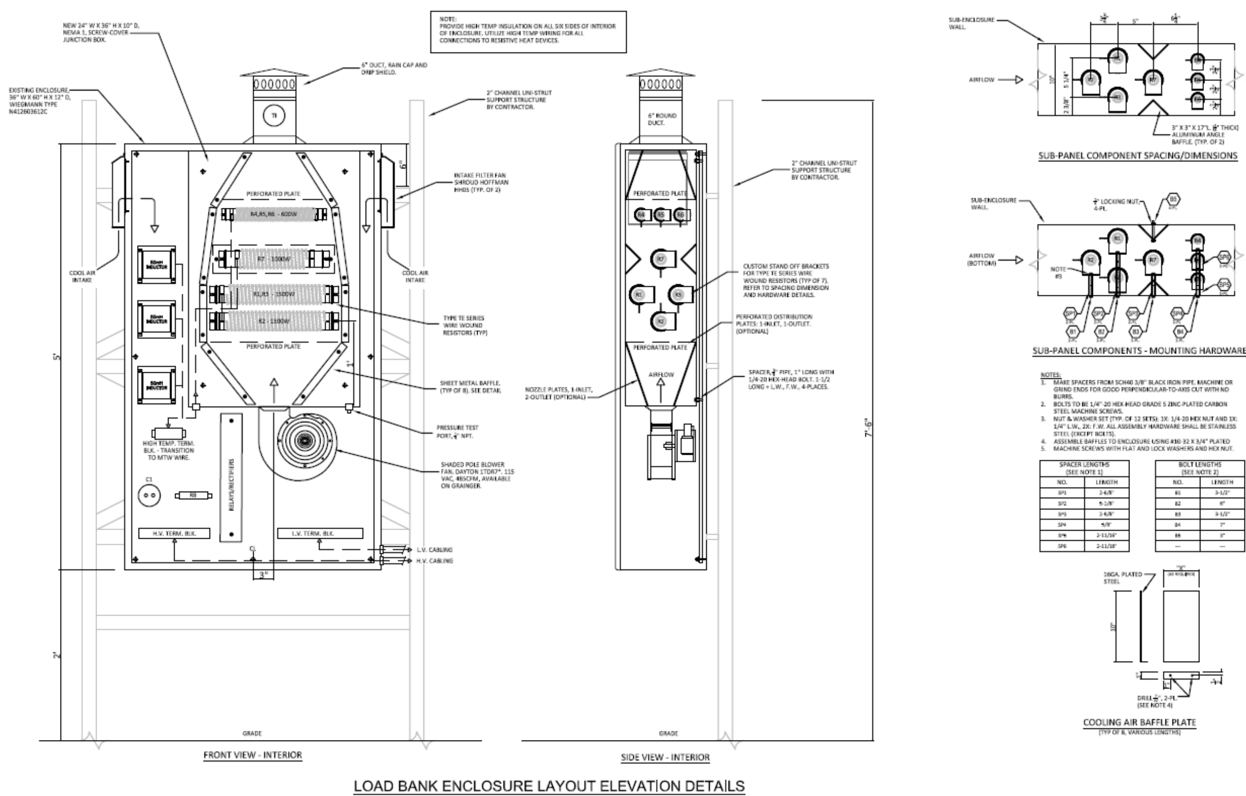


*Figure 8: Load Bank Enclosure*

The capstone team selected a a 36” x 60” x 12”  outdoor electrical enclosure to house the Programmable Load, which is made up of the load bank resistors, a bridge rectifier, switching relays/contactors, an air circulation blower fan, power and controls cabling and terminal blocks, etc. The Enclosure is NEMA 4 rated to provide a weather-proof seal to protect internal electronic components. An internal back plate/panel shall be included within the enclosure for mounting of electrical components. The diagrams of the physical implementation of all these components in the control and load enclosures has been generated in AutoCAD as shown in figure 8. At this point, we are working to fabricate all these components in the enclosures.

## 9. Control Scheme Design and Validation

The main purpose of the control design process is to design a controller that can manage different load combinations for the Grid-Emulating inverter and PV inverter. Firstly, a linear PI dual loop controller has been designed and applied to the Grid-Emulating inverter. The current controller is the inner loop, and the voltage controller is the outer loop. The voltage outer loop is used to generate the reference current to the current inner loop. The controllers have been implemented using PLECS toolbox and Simpowersystem (MATLAB/SIMULINK) software. Different load conditions have been used to test the controller, and the simulation results are summarized in the Table 5.

From this table, we can note that the controller has a very good response for a balanced resistive load. The THD in this case is equal to 0.35%, and the steady state voltage error is equal to 0.16[$V_p$]. In the case of the resistive-inductive load, the THD increased to 1.2%, and the steady state error also increased to 1.87[Vp]. Even though these values have increased, they are still acceptable.

To test the controller under a nonlinear load, a full bridge rectifier with ultra-high crest factor has been used. From the simulation results, we can note that the performance of the proposed linear controller is bad since the THD is 5.9% and the steady state error is 14 V.

*Table 3*

| Grid-Emulating Inverter (GEI) | GEI Mode | RL-Load | R-Load | NL-Load | THD% | SSR(V) |
|---|---|---|---|---|---|---|
| Active | Dual Level Control | 0 | 3 | 0 | 0.35 | 0.16 |
| Active | Dual Level Control | 3 | 0 | 0 | 1.2 | 1.87 |
| Active | Dual Level Control | 0 | 0 | 1 | 5.9 | 14 |

Based on the results of the linear PI controller, our contribution will be to apply nonlinear control methods and include the uncertainties, disturbances, time-delays, and unknowns as part of our solutions.

Secondly, the PV inverter has been implemented on the same software, and the process of the controller design has been started. In the PV inverter case, the process is more complicated than in the case of the Grid-Emulating inverter. This complexity comes from the fact that we need to control many more variables. Reactive power, active power, power factor, and maximum power point tracking should be considered in the control design. In the linear control theory, we need to design the controller for each variable, but in the nonlinear control arena, we are trying to design one controller that can deal with all of these objectives.

Thirdly, the Grid-Emulating inverter and PV inverter should be connected in parallel to share the total loads. This stage will be more challenging because we have to control the shared power between the inverters.

Lastly, the set of the two inverters may be connected to the grid, so the control system should have the ability to seamless transition from standalone operation to grid-connected operation. To do that, the frequency and phase of the inverters should be changed to match those of the grid.

## 10. Conclusions and Future Work

The micro-grid system shows promise as its development continues. The proposed test bed will be extremely useful for demonstrating renewable energy integration to an AC grid environment.

The primary work that is to be completed next is the fabrication and installation of the physical test bed. With respect to the Low-Level PCB development effort we have first pieced prototyped our four PCB system with success. We are currently waiting on our second revision of PCB3 and PCB4 to complete our fabrication of this system. In our lab, we are fabricating the Control Enclosure along with the Load Bank Enclosure. We have procured 100% of the bill of material items and are working to finalize the laboratory demonstration of the system within 1 month. In parallel with this effort our graduate students are have an initial program in the NI LabView platform for the low level control of the Grid-Emulating Inverter along with the system level control of the Control Enclosure contacts for testing on of the three loads. Once we have these first demonstration test completed we will move quickly to test the various loads. To test the system under PV excitation we will need to move the test bed to the Phoenix house and connect the string of PV modules to the system. The final phase of the project will begin when the test-bed is fully functional. At that point, the educational modules will be created which will demonstrate the following concepts to our students: grid synchronization, MPPT for PV arrays, Power Factor Correction, and compensation for nonlinear and unbalanced loads.

## 11. Acknowledgement

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